

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2000-124007

(43)Date of publication of application : 28.04.2000

(51)Int.Cl.

H01C 7/04

H01C 17/30

(21)Application number : 10-290803

(71)Applicant : MURATA MFG CO LTD

(22)Date of filing : 13.10.1998

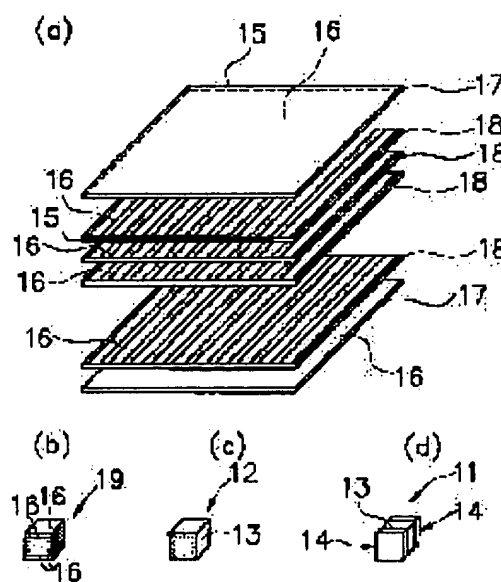
(72)Inventor : FURUKAWA NOBORU
KAWASE MASAHIKO
ITO YASUNORI

(54) CHIP THERMISTOR AND METHOD OF PRODUCING THE SAME

(57)Abstract:

PROBLEM TO BE SOLVED: To prevent the deterioration of strength resistant to break and reliability by forming external electrodes at both ends of a thermistor element, and forming a diffused layer of high resistivity inorganic material which is different from the thermistor element material near the exposed external surface of the thermistor element.

SOLUTION: In a chip thermistor 11, a predetermined number of inner layer green sheets 18 are laminated, the external green sheets 17 are placed on and under a group of the inner layer green sheets as the upper layer and the lower layer, respectively, a group of sheets are attached one another by a hydraulic press so as to be at a specified thickness and are integrated. The upper external green sheet and the lower external green sheet 17 are then laminated so that their glass paste 16 coating face face opposite adjacent inner green sheets 18. In addition, the formed body is cut into a prescribed chip shape at a predetermined cutting position, so that glass paste 16 printed on the inner green sheet 18 is positioned on each of opposite faces of a chip body 19. The chip body 19 is fired at 1,000-1,300°C, and diffused layers 13 are formed on four sides of the chip body.



BEST AVAILABLE COPY

LEGAL STATUS

[Date of request for examination] 10.07.2000
[Date of sending the examiner's decision of rejection]
[Kind of final disposal of application other than the
examiner's decision of rejection or application
converted registration]
[Date of final disposal for application]
[Patent number] 3368845
[Date of registration] 15.11.2002
[Number of appeal against examiner's decision of
rejection]
[Date of requesting appeal against examiner's
decision of rejection]
[Date of extinction of right]

Copyright (C); 1998,2003 Japan Patent Office

(19) 日本国特許庁 (JP)

(12) 公開特許公報 (A)

(11) 特許出願公開番号

特開 2000-124007

(P 2000-124007A)

(43) 公開日 平成12年4月28日 (2000. 4. 28)

(51) Int. Cl. 7

識別記号

F I

テーマコード (参考)

H 0 1 C 7/04
17/30H 0 1 C 7/04
17/305E032
5E034

審査請求 未請求 請求項の数 5

O L

(全 6 頁)

(21) 出願番号 特願平10-290803

(22) 出願日 平成10年10月13日 (1998. 10. 13)

(71) 出願人 000006231

株式会社村田製作所

京都府長岡京市天神二丁目26番10号

(72) 発明者 古川 昇

京都府長岡京市天神二丁目26番10号 株式
会社村田製作所内

(72) 発明者 川瀬 政彦

京都府長岡京市天神二丁目26番10号 株式
会社村田製作所内

(72) 発明者 井藤 恭典

京都府長岡京市天神二丁目26番10号 株式
会社村田製作所内

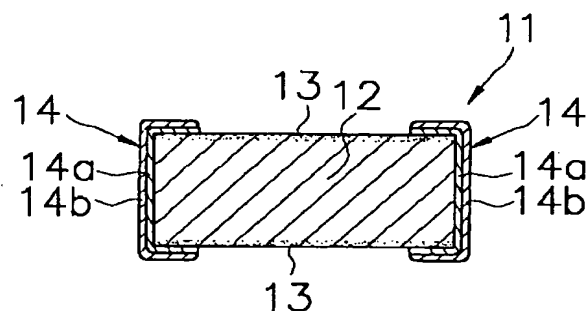
最終頁に続く

(54) 【発明の名称】 チップ型サーミスタおよびその製造方法

(57) 【要約】

【課題】 表面を絶縁化した新規な構造のチップ型サーミスタおよびその製造方法を提供する。

【解決手段】 サーミスタ素子の両端部に外部電極が形成されており、外部露出しているサーミスタ素子の外表面近傍に、サーミスタ素子材料以外の高比抵抗無機物の拡散層が形成されている。



【特許請求の範囲】

【請求項 1】 サーミスタ素子の両端部に外部電極が形成されており、外部露出しているサーミスタ素子の外表面近傍に、サーミスタ素子材料以外の高比抵抗無機物の拡散層が形成されていることを特徴とするチップ型サーミスタ。

【請求項 2】 前記外部電極が電解メッキ層からなることを特徴とする請求項 1 記載のチップ型サーミスタ。

【請求項 3】 サーミスタ用セラミックグリーンシートを準備する工程と、

このセラミックグリーンシートの切断予定位置を含む領域に無機物を塗布する工程と、

前記セラミックグリーンシートを所定枚数積層する工程と、

この積層体を切断予定位置でチップ状に切断、焼成する工程と、

この焼成体の両端部に外部電極を形成する工程と、を備えることを特徴とするチップ型サーミスタの製造方法。

【請求項 4】 前記無機物を塗布した最上層と最下層のセラミックグリーンシートは、無機物塗布面が隣接するセラミックグリーンシートと向かい合うように積層されることを特徴とする請求項 3 記載のチップ型サーミスタの製造方法。

【請求項 5】 前記外部電極を形成する工程は、前記焼成体を電解メッキし、この焼成体の両端部に電解メッキ層を形成することを特徴とする請求項 3 記載のチップ型サーミスタの製造方法。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】この発明は、表面実装用チップ型サーミスタ、特に、電子機器の温度補償用や表面温度測定センサとして用いられるチップ型サーミスタとその製造方法に関するものである。

【0002】

【従来の技術】チップ型サーミスタは、外部電極に電解メッキを施す場合、サーミスタ素子の露出面が腐食、溶解して、抵抗値変化を生じるという問題がある。したがって、チップ型サーミスタは、サーミスタ素子表面にガラス層などの絶縁層を形成し、電解メッキ時のサーミスタ素子の腐食を防止している。

【0003】例えば、特開平 3-250603 号公報には、図 7 に示すようなチップ型サーミスタ 1 が開示されている。チップ型サーミスタ 1 は、両端部を除く表面がガラス層 3 で被覆されたサーミスタ素子 2 の両端部に外部電極層 4、4 が形成されたものである。

【0004】このチップ型サーミスタ 1 は、図 8 に示すような製造方法で作製される。図 8 (a) に示すように、セラミックグリーンシートの両主面にガラスペーストを印刷して焼付け、サーミスタ素体 5 の両主面にガラス層 3 を形成する。この焼結シート 6 を、ダイシングソ

ウで短冊状に切断した後、その切断面にもガラスペーストを印刷、焼付けして、図 8 (b) に示すように切断面にもガラス層 3 を形成する。さらに、この短冊状物 7 を前記切断面と垂直な方向に切断して、図 8 (c) に示すようなチップ状のサーミスタ素子 2 を得る。

【0005】このサーミスタ素子 2 の切断面である両端部に導電性ペーストを塗布、焼付けて、焼付け電極層 4 a、4 a を形成する。さらに、焼付け電極層 4 a、4 a の上に、電解メッキ法によりメッキ層 4 b、4 b を形成することにより、図 8 (d) に示すようなチップ型サーミスタ 1 を得る。

【0006】

【発明が解決しようとする課題】しかしながら、このようなチップ型サーミスタ 1 の製造方法は、両主面にガラス層 3 が形成された焼結シート 6 をダイシングソウで切断する工程や、その後再び、露出した切断面にガラスペーストを焼付ける工程が必要であり、工程が複雑でコストが高いという問題があった。

【0007】この発明の目的は、表面を絶縁化した新規な構造のチップ型サーミスタおよびその製造方法を提供することである。

【0008】

【課題を解決するための手段】この発明に係るチップ型サーミスタは、サーミスタ素子の両端部に外部電極が形成されており、外部露出しているサーミスタ素子の外表面近傍に、サーミスタ素子材料以外の高比抵抗無機物の拡散層が形成されていることを特徴とする。

【0009】前記外部電極は電解メッキ層からなることが好ましい。

【0010】この発明に係るチップ型サーミスタの製造方法は、サーミスタ用セラミックグリーンシートを準備する工程と、このセラミックグリーンシートの切断予定位置を含む領域に無機物を塗布する工程と、前記セラミックグリーンシートを所定枚数積層する工程と、この積層体を切断予定位置でチップ状に切断、焼成する工程と、この焼成体の両端部に外部電極を形成する工程と、を備えることを特徴とする。

【0011】前記無機物を塗布した最上層と最下層のセラミックグリーンシートは、無機物塗布面が隣り合うセラミックグリーンシートと向かい合うように積層されることが好ましい。

【0012】前記外部電極を形成する工程は、前記焼成体を電解メッキし、この焼成体の両端部に電解メッキ層を形成することが好ましい。

【0013】これらの発明によれば、グリーンシートに無機物を印刷する工程だけで、サーミスタ素子表面を絶縁化したチップ型サーミスタを得ることができる。

【0014】

【発明の実施の形態】この発明における一つの実施の形態について、図 1 および図 2 に基づいて、詳細に説明す

る。

【0015】図1に示すチップ型サーミスタ11は、サーミスタ素子12と、このサーミスタ素子12の両端部を除く外表面近傍に形成された拡散層13と、サーミスタ素子12の両端部に形成された外部電極14、14とからなる。

【0016】このチップ型サーミスタ11は、以下の製造方法にて作製される。まず、例えば、Mn、Ni、Co、Fe、Cu、Alから選ばれる2以上の金属からなる酸化物を主成分とするサーミスタ用原料に、有機バインダー、分散材、表面活性材、消泡材、溶剤を所定量加え、40～60μmのグリーンシート15を作製し、所定サイズにカットする。次に、このグリーンシート15の一主面にほうけい酸亜鉛を主成分とするガラスペースト16を印刷して外層用グリーンシート17を作製する。さらに、グリーンシート15の一主面の切断予定位置を含む領域に、上記ガラスペースト16を所定間隔ずつ離して線状に印刷して内層用グリーンシート18を作製する。

【0017】次に、図2(a)に示すように、内層用グリーンシート18を所定枚数積層し、その上下に最上層と最下層の外層用グリーンシート17を重ねて、所定厚みになるように油圧プレス機で圧着し、一体化する。このとき、最上層と最下層の外層用グリーンシート17は、ガラスペースト16塗布面が隣接する内層用グリーンシート18に向かい合うように、つまり、ガラスペースト16塗布面が外部に露出しないように重ねる。さらに、その成形体を、図2(b)に示すように、内層用グリーンシート18に印刷したガラスペースト16がチップ体19の対抗する両側面に配置されるよう、切断予定位置で所定サイズのチップ形状に切断する。このチップ体19を1000～1300℃で焼成して、図2(c)に示すような4側面に拡散層13が形成されたサーミスタ素子12を得る。

【0018】すなわち、チップ体19を焼成することにより、チップ体19の上下最外層のガラスペースト16と、チップ体19の両側面に露出した層状のガラスペースト16とが拡散して、サーミスタ素子12の4側面近傍に拡散層13が形成される。チップ体19の両側面に露出した層状のガラスペースト16の拡散が不十分な場合は、拡散層13が両側面一面に形成されずに多層状の拡散層になるが、この場合でも一定の絶縁効果は得られるため、実用上問題は無い。

【0019】なお、積層した内層用グリーンシート18の上下に外層用グリーンシート17を重ねる際、外層用グリーンシート17のガラスペースト16塗布面を内側に向けて重ねるのは、焼成時にガラスペースト16が熔融してチップ体19同士がくっついたり、チップ体19が匣にくっつくのを防止するためである。つまり、ガラスペースト16塗布面が外側に露出していると、焼成時

にガラスペースト16が熔融してチップ体19同士がくっついたり、チップ体19が匣にくっつくことがある。このようなくっつきが問題にならない場合は、ガラスペースト16塗布面が外側に露出するように積み重ねてもよい。

【0020】次に、このサーミスタ素子12の両端部に、下地層としてAgからなる外部電極ペーストを塗布、焼付けし、焼付け電極層14a、14aを形成する。さらに焼付け電極層14a、14a上に電解メッキ法により、Ni、Snの2層からなるメッキ層14b、14bを形成して、チップ型サーミスタ11を得る。

【0021】したがって、チップ型サーミスタ11は、セラミックグリーンシート15の積層方向に対して外部電極14、14形成面が垂直方向になる。

【0022】また、この発明のチップ型サーミスタ11においては内部電極の有無は問わないが、内層用グリーンシート18の積層前に、必要に応じて内層用グリーンシート18の表面に内部用の電極を形成し、サーミスタ素子12内部に電極を形成したものであってもよい。

【0023】なお、拡散層13は、必ずしもサーミスタ素子12の4側面全面に形成する必要はなく、図3に示すように、外部電極形成部を除くサーミスタ素子12aの外表面近傍に形成されていればよい。サーミスタ素子12aのセラミックグリーンシート15の積層状態は、図4に示すようなものである。すなわち、外層用グリーンシート17aには外部電極形成部を除くように、セラミックグリーンシート15の両端部を除いて帯状にガラスペースト16が塗布される。内層用グリーンシート18aにはセラミックグリーンシート15の両端部を除いて両側縁にガラスペースト16が塗布される。

【0024】これら外層用グリーンシート17a、内層用グリーンシート18aを所定枚数積層し、焼成することにより、サーミスタ素子12aを得ることができる。

【0025】さらに、サーミスタ素子12の外表面近傍に形成される拡散層は、必ずしもガラスである必要はなく、ガラスペーストに変えて、例えばAl、Si、Ti、Sn等の3価以上の金属酸化物、又はZn、Al、W、Zr、Sb、Y、Sm、Ti、Feの少なくとも1種以上を含有するサーミスタ素子よりも高比抵抗の材料を塗布し、圧着、焼成してもよい。これにより、高比抵抗材料が拡散されて、サーミスタ素子12の外表面近傍が絶縁化または高比抵抗化される。

【0026】次に、この発明における他の実施の形態について、図5に基づいて説明する。なお、チップ型サーミスタ11と同一のものについては同一の符号を付し、詳細な説明を省略する。

【0027】チップ型サーミスタ11bは、外観上、サーミスタ素子12aと同一のサーミスタ素子12bを有し、このサーミスタ素子12bの外表面近傍に形成された拡散層13と、サーミスタ素子12bの両端部に形成

された外部電極 14、14 とからなる。

【0028】チップ型サーミスタ 11b は、以下の製造方法で作製される。まず、チップ型サーミスタ 11 と同様のグリーンシート 15 を準備し、所定サイズにカットする。次に、グリーンシート 15 の一主面の切断予定位置を含む領域に、ほうけい酸亜鉛を主成分とするガラスペースト 16 を四角形を切り欠いた棧状に塗布して内層用グリーンシート 18b を作製する。

【0029】次に、図 5 (a) に示すように、内層用グリーンシート 18a を所定枚数積層し、その上下にグリーンシート 15 を重ねて、所定厚みになるように油圧プレス機で圧着し、一体化する。その成形体を、図 5

(b) に示すように、内層用グリーンシート 18b に印刷したガラスペースト 16 がチップ体 19b の 4 側縁に配置されるよう、所定サイズのチップ形状に切断する。このチップ体 19b を 1000 ~ 1300℃ で焼成して、図 5 (c) に示すような、4 側面近傍に拡散層 13 が形成されたサーミスタ素子 12b を得る。

【0030】すなわち、チップ体 19b を焼成することにより、チップ体 19b の 4 側面に露出するように形成された層状のガラスペースト 16 が拡散して、サーミスタ素子 12b の 4 側面を被覆するように拡散層 13 が形成される。

【0031】次に、このサーミスタ素子 12b の両端部、この場合は拡散層 13 が形成されていない上下最外層の両主面を含めて、下地層として Ag からなる外部電極ペーストを塗布、焼付けし、焼付け電極層 14a、14a を形成する。さらに焼付け電極層 14a、14a 上に電解メッキ法により、Ni、Sn の 2 層からなるメッキ層 14b、14b を形成して、チップ型サーミスタ 11b を得る。

【0032】したがって、チップ型サーミスタ 11b は、グリーンシート 15 の積層方向に対して外部電極 14、14 形成面が平行である。

【0033】なお、チップ型サーミスタ 11b に内部電極を形成する方法としては、例えば、内層用グリーンシートの所定の位置に貫通孔を設け、この貫通孔に導体ペーストを充填する方法がある。すなわち、図 6 (a) に基づいてチップ状のサーミスタ素子 12c 1 個分について説明すると、まず、4 側縁にガラスペーストが塗布された内層用グリーンシート 18b に所定面積の内部電極 20 を形成して内層用グリーンシート 18c を作製する。次に、内層用グリーンシート 18b に貫通孔 21 を形成し、その貫通孔 21 に導体ペーストを充填した内層用グリーンシート 18d を作製する。そして、内層用グリーンシート 18c を所定距離だけ離して重ね、その上下に内層用グリーンシート 18d を所定枚数積層する。

さらに、上下最外層には、内層用グリーンシート 18d と同様に貫通孔 21 に導体ペーストを充填したグリーンシート 15a を重ねる。この積層体を圧着、焼成することにより、図 6 (b) に示すように、4 側面近傍に拡散層 13 が形成され、内部に外部電極 14、14 形成面と平行に形成された内部電極 20、20 が、外部電極 14、14 と接続されるように、サーミスタ素子 12c の両端面まで引き出されたサーミスタ素子 12c を得ることができる。

【0034】なお、チップ型サーミスタ 11、11b の外部電極 14、14 は、サーミスタ素子 12、12b の組成に適宜して、例えば、Mn、Ni、Co、Fe、Cu、Al の 2 種以上からなる酸化物を主成分とする比抵抗が 200 Ω・cm 以下のセラミックからなる場合、下地層である焼付け電極層 14a、14a を省略し、サーミスタ素子 12、12b に直接電解メッキ法によりメッキ層 14b、14b を形成してもよい。

【0035】上記のチップ型サーミスタ 11、11b を準備し、さらに比較例として拡散層 13 を形成していないチップ型サーミスタを準備し、電解メッキによる抵抗変化率と抵抗バラツキを調べた。その結果を表 1 に表す。なお、実施例 1 はチップ型サーミスタ 11、実施例 2 はチップ型サーミスタ 11b である。

【0036】

【表 1】

	拡散層	メッキによる 抵抗変化率(%)	抵抗バラツキ 3 CV(%)
実施例 1	有	ΔR=0.05	6.5
実施例 2	有	ΔR=0.1	6.6
比較例 3	無	ΔR=3.5	7.5

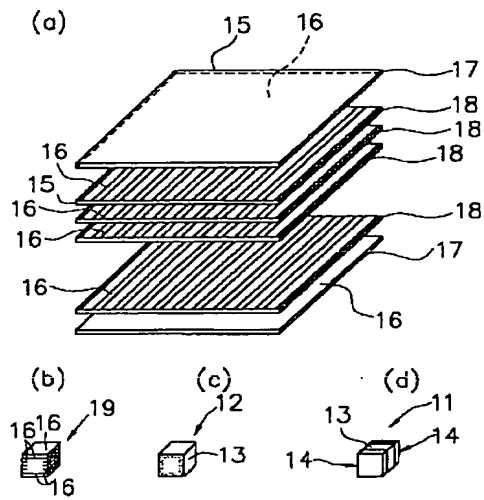
【0037】表 1 に示すように、拡散層 13 を形成したチップ型サーミスタ 11、11b は、メッキによる抵抗率変化が 0.05%、0.01% と非常に小さい。また、抵抗値のばらつきを示す 3 CV も小さいことがわかる。

【0038】次に、実施例 1、2 のチップ型サーミスタ 11、11b の抗折強度を調べた。さらに、ライフ放置試験を行い、高温、低温もしくは高温中での抵抗値や B 定数の変化を調べた。同様に、比較例のチップ型サーミスタについても調べ、比較した。なお、放置試験は、125℃、60℃・95%RH、-40℃でそれぞれ 1000 時間放置したときの抵抗値の変化率を調べたものである。その結果を表 2 に表す。

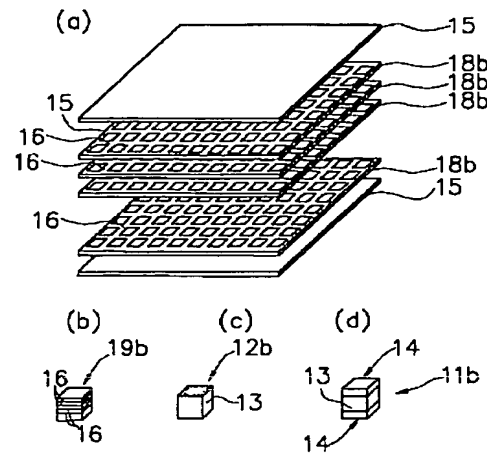
【0039】

【表 2】

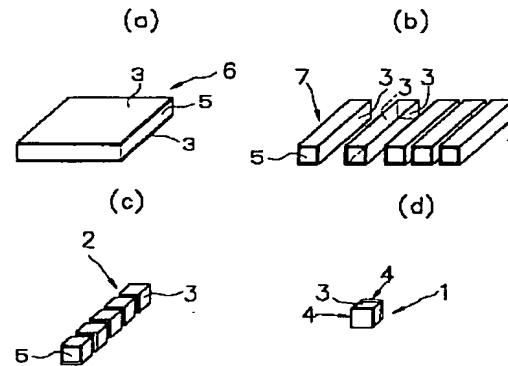
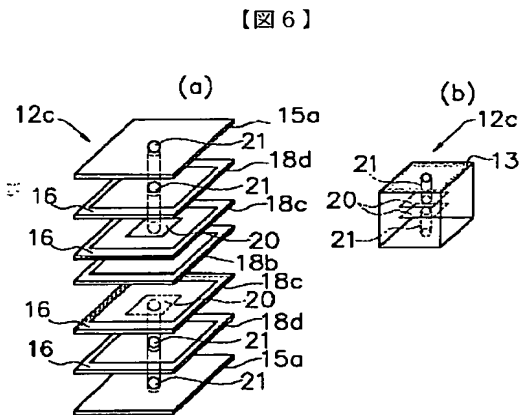
【図2】



【図5】



【図8】



フロントページの続き

Fターム(参考) 5E032 AB10 BA23 BB10 CA02 CC14
CC16
5E034 BA09 BB01 DB13 DB17 DC01
DC03 DC09 DE07 DE16 DE17

* NOTICES *

JPO and NCIP are not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3. In the drawings, any words are not translated.

CLAIMS

[Claim(s)]

[Claim 1] The chip mold thermistor characterized by forming the external electrode in the both ends of a thermistor component, and forming the diffusion layer of high specific resistance inorganic substances other than a thermistor component ingredient near the outside surface of the thermistor component which is carrying out external exposure.

[Claim 2] The chip mold thermistor according to claim 1 characterized by said external electrode consisting of an electrolysis deposit.

[Claim 3] The manufacture approach of the chip mold thermistor characterized by to have the process for which the ceramic green sheet for thermistors is prepared, the process which applies an inorganic substance to a field including the cutting predetermined position of this ceramic green sheet, the process which carries out the predetermined number-of-sheets laminating of said ceramic green sheet, the process which cut this layered product to the shape of a chip in a cutting predetermined position, and are calcinated, and the process which form an external electrode in the both ends of this baking object.

[Claim 4] The ceramic green sheet of the maximum upper layer and the lowest layer which applied said inorganic substance is the manufacture approach of the chip mold thermistor according to claim 3 characterized by carrying out a laminating so that the ceramic green sheet with which an inorganic substance spreading side adjoins may be faced.

[Claim 5] The process which forms said external electrode is the manufacture approach of the chip mold thermistor according to claim 3 which carries out electrolytic plating of said baking object, and is characterized by forming an electrolysis deposit in the both ends of this baking object.

[Translation done.]

* NOTICES *

JPO and NCIPI are not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3. In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to the chip mold thermistor for surface mounts, the chip mold thermistor especially used as the object for temperature compensations and skin temperature measurement sensor of electronic equipment, and its manufacture approach.

[0002]

[Description of the Prior Art] When performing electrolytic plating to an external electrode, the exposure of a thermistor component corrodes and dissolves, and a chip mold thermistor has the problem of producing a change in resistance. Therefore, the chip mold thermistor formed insulating layers, such as a glass layer, in the thermistor component front face, and has prevented the corrosion of the thermistor component at the time of electrolytic plating.

[0003] For example, the chip mold thermistor 1 as shown in drawing 7 is indicated by JP, 3-250603, A. The external electrode layers 4 and 4 are formed in the both ends of the thermistor component 2 to which the front face excluding [the chip mold thermistor 1] both ends was covered with the glass layer 3.

[0004] This chip mold thermistor 1 is produced by the manufacture approach as shown in drawing 8. As shown in drawing 8 (a), a glass paste is printed and baked on both the principal planes of a ceramic green sheet, and the glass layer 3 is formed in both the principal planes of the thermistor element assembly 5. After a dicing saw cuts this sintering sheet 6 in the shape of a strip of paper, a glass paste is printed also to that cutting plane, and it burns to it, and as shown in drawing 8 (b), the glass layer 3 is formed also in a cutting plane. Furthermore, this strip-of-paper-like object 7 is cut in the direction perpendicular to said cutting plane, and the thermistor component 2 of

the shape of a chip as shown in drawing 8 (c) is obtained.

[0005] A conductive paste is applied and baked on the both ends which are the cutting planes of this thermistor component 2, and the printing electrode layers 4a and 4a are formed. Furthermore, the chip mold thermistor 1 as shown in drawing 8 (d) is obtained by forming deposits 4b and 4b with electrolysis plating on the printing electrode layers 4a and 4a.

[0006]

[Problem(s) to be Solved by the Invention] However, such a manufacture approach of the chip mold thermistor 1 had the problem that the process which bakes a glass paste on the cutting plane exposed again was required, a process was complicated, and cost was high, the process which cuts the sintering sheet 6 with which the glass layer 3 was formed in both principal planes with a dicing saw, and after that.

[0007] The purpose of this invention is offering the chip mold thermistor and its manufacture approach of the new structure which insulation-ized the front face.

[0008]

[Means for Solving the Problem] The chip mold thermistor concerning this invention is characterized by forming the external electrode in the both ends of a thermistor component, and forming the diffusion layer of high specific resistance inorganic substances other than a thermistor component ingredient near the outside surface of the thermistor component which is carrying out external exposure.

[0009] As for said external electrode, consisting of an electrolysis deposit is desirable.

[0010] The manufacture approach of the chip mold thermistor concerning this invention is characterized by to have the process for which the ceramic green sheet for thermistors is prepared, the process which applies an inorganic substance to a field including the cutting predetermined position of this ceramic green sheet, the process which carries out the predetermined number-of-sheets laminating of said ceramic green sheet, the process which cuts this layered product to the shape of a chip in a cutting predetermined position, and calcinate, and the process which form an external electrode in the both ends of this baking object.

[0011] As for the ceramic green sheet of the maximum upper layer and the lowest layer which applied said inorganic substance, it is desirable that a laminating is carried out so that the ceramic green sheet with which an inorganic substance spreading side adjoins each other may be faced.

[0012] As for the process which forms said external electrode, it is desirable to carry out electrolytic plating of said baking object, and to form an electrolysis deposit in the both ends of this baking object.

[0013] According to these invention, the chip mold thermistor which insulation-ized the thermistor component front face can be obtained only at the process which prints an inorganic substance to a green sheet.

[0014]

[Embodiment of the Invention] The gestalt of one operation in this invention is explained to a detail based on drawing 1 and drawing 2 .

[0015] The chip mold thermistor 11 shown in drawing 1 consists of the thermistor component 12, a diffusion layer 13 formed near the outside surface except the both ends of this thermistor component 12, and external electrodes 14 and 14 formed in the both ends of the thermistor component 12.

[0016] This chip mold thermistor 11 is produced by the following manufacture approaches. First, specified quantity **** and the 40-60-micrometer green sheet 15 are produced in the raw material for thermistors which uses as a principal component the oxide which consists of two or more metals chosen from Mn, nickel, Co, Fe, Cu, and aluminum, for example, and an organic binder, distributed material, a surface active agent, defoaming material, and a solvent are cut into it at predetermined size. Next, the glass paste 16 which uses way silicic-acid zinc as a principal component at one principal plane of this green sheet 15 is printed, and the green sheet 17 for outer layers is produced. Furthermore, to a field including the cutting predetermined position of one principal plane of a green sheet 15, the above-mentioned glass paste 16 is detached predetermined spacing every, it prints to a line, and the green sheet 18 for inner layers is produced.

[0017] Next, as shown in drawing 2 (a), the predetermined number-of-sheets laminating of the green sheet 18 for inner layers is carried out, in piles, with a hydraulic press machine, it is stuck by pressure and the green sheet 17 for outer layers of the maximum upper layer and the lowest layer is united with the upper and lower sides so that it may become predetermined thickness. At this time, the green sheet 17 for outer layers of the maximum upper layer and the lowest layer is piled up so that a glass paste 16 spreading side may not be outside exposed, so that the green sheet 18 for inner layers with which a glass paste 16 spreading side adjoins may be faced that is,. Furthermore, as shown in drawing 2 (b), the Plastic solid is cut in the chip configuration of predetermined size in a cutting predetermined position so that the glass paste 16 printed to the green sheet 18 for inner layers may be arranged

in the both-sides side where the chip object 19 opposes. This chip object 19 is calcinated at 1000-1300 degrees C, and the thermistor component 12 by which the diffusion layer 13 was formed in four side faces as shown in drawing 2 (c) is obtained.

[0018] That is, by calcinating the chip object 19, the glass paste 16 of the vertical outermost layer of the chip object 19 and the layer-like glass paste 16 exposed to the both-sides side of the chip object 19 are spread, and a diffusion layer 13 is formed near the 4 side faces of the thermistor component 12. When diffusion of the layer-like glass paste 16 exposed to the both-sides side of the chip object 19 is inadequate, a diffusion layer 13 turns into a multilayer diffusion layer, without being formed in a both-sides flat-tapped side, but since the fixed insulating effectiveness is acquired even in this case, it is satisfactory practically.

[0019] In addition, in case [of the green sheet 18 for inner layers which carried out the laminating] the green sheet 17 for outer layers is piled up up and down, the glass paste 16 spreading side of the green sheet 17 for outer layers is turned and piled up inside for preventing that the glass paste 16 fuses at the time of baking, chip object 19 comrades adhere or the chip object 19 adheres to **. That is, when the glass paste 16 spreading side is outside exposed, the glass paste 16 fuses at the time of baking, chip object 19 comrades may adhere or the chip object 19 may adhere to **. When not becoming a problem with ** that there is nothing in this way, you may put so that a glass paste 16 spreading side may be outside exposed.

[0020] Next, the external electrode paste which consists of Ag as a substrate layer is applied and burned to the both ends of this thermistor component 12, and the printing electrode layers 14a and 14a are formed in them. Furthermore it bakes, the deposits 14b and 14b which consist of two-layer [of nickel and Sn] with electrolysis plating on electrode layer 14a and 14a are formed, and the chip mold thermistor 11 is obtained.

[0021] Therefore, as for the chip mold thermistor 11, the external electrode 14 and 14 forming faces become perpendicularly to the direction of a laminating of the ceramic green sheet 15.

[0022] Moreover, although the existence of an internal electrode does not ask in the chip mold thermistor 11 of this invention, in front of the laminating of the green sheet 18 for inner layers, the electrode for the interior may be formed on the front face of the green sheet 18 for inner layers, and an electrode may be formed in the thermistor component 12 interior if needed.

[0023] In addition, it is not necessary to necessarily form a diffusion layer 13 all over 4 side faces of the thermistor component 12, and as shown in drawing 3 , it should just be formed near the outside surface of thermistor component 12a except the external electrode formation section. It seems that the laminating condition of the ceramic green sheet 15 of thermistor component 12a is shown in drawing 4 . That is, except for the both ends of the ceramic green sheet 15, the glass paste 16 is applied to band-like so that the external electrode formation section may be removed to green sheet 17for outer layers a. Except for the both ends of the ceramic green sheet 15, the glass paste 16 is applied to edges on both sides at green sheet 18for inner layers a.

[0024] Thermistor component 12a can be obtained by carrying out the predetermined number laminating of green sheet 17for these outer layers a, and the green sheet 18a for inner layers, and calcinating them.

[0025] Furthermore, the diffusion layer formed near the outside surface of the thermistor component 12 does not necessarily need to be glass, and may apply and stick by pressure and calcinate the ingredient of high specific resistance rather than the thermistor component which changes into a glass paste, for example, contains at least one or more sorts of the metallic oxide more than trivalent [, such as aluminum, Si, Ti, and Sn,], or Zn, aluminum, W, Zr, Sb, Y, Sm, Ti and Fe. thereby, a high specific resistance ingredient is spread -- having -- the near outside surface of the thermistor component 12 -- insulation-izing -- or high specific resistance is formed.

[0026] Next, the gestalt of other operations in this invention is explained based on drawing 5 . In addition, the sign same about the same thing as the chip mold thermistor 11 is attached, and detailed explanation is omitted.

[0027] Chip mold thermistor 11b has the same thermistor component 12b as an exterior and thermistor component 12a, and consists of a diffusion layer 13 formed near the outside surface of this thermistor component 12b, and external electrodes 14 and 14 formed in the both ends of thermistor component 12b.

[0028] Chip mold thermistor 11b is produced by the following manufacture approaches. First, the same green sheet 15 as the chip mold thermistor 11 is prepared, and it cuts into predetermined size. next, the crosspiece which turned off the square to the field including the cutting predetermined position of one principal plane of a green sheet 15, and lacked to it the glass paste 16 which uses way silicic-acid zinc as a principal component -- it applies to a ** and green sheet 18b for inner layers is produced.

[0029] Next, as shown in drawing 5 (a), the predetermined number-of-sheets laminating of the green sheet 18a for inner layers is carried out, in piles, with a hydraulic press machine, it is stuck by pressure and a green sheet 15 is united with the upper and lower sides so that it may become predetermined thickness. As shown in drawing 5 (b), the Plastic solid is cut in the chip configuration of predetermined size so that the glass paste 16 printed to green sheet 18b for inner layers may be arranged at four side edges of chip object 19b. This chip object 19b is calcinated at 1000-1300 degrees C, and thermistor component 12b in which the diffusion layer 13 was formed near the 4 side faces as shown in drawing 5 (c) is obtained.

[0030] That is, by calcinating chip object 19b, the glass paste 16 of the shape of a layer formed so that it might expose to four side faces of chip object 19b is spread, and a diffusion layer 13 is formed so that four side faces of thermistor component 12b may be covered.

[0031] Next, the external electrode paste including the both ends of this thermistor component 12b and both the principal planes of the vertical outermost layer in which the diffusion layer 13 is not formed in this case which consists of Ag as a substrate layer is applied and burned, and the printing electrode layers 14a and 14a are formed. Furthermore it bakes, the deposits 14b and 14b which consist of two-layer [of nickel and Sn] with electrolysis plating on electrode layer 14a and 14a are formed, and chip mold thermistor 11b is obtained.

[0032] Therefore, chip mold thermistor 11b has the external electrode 14 and 14 parallel forming faces to the direction of a laminating of a green sheet 15.

[0033] In addition, as an approach of forming an internal electrode in chip mold thermistor 11b, a through tube is prepared in the position of the green sheet for inner layers, and there is the approach of filling up this through tube with conductive paste, for example. That is, if 12c1 chip-like thermistor component is explained based on drawing 6 (a), the internal electrode 20 of predetermined area will be first formed in green sheet 18b for inner layers by which the glass paste was applied to four side edges, and green sheet 18c for inner layers will be produced. Next, a through tube 21 is formed in green sheet 18b for inner layers, and green sheet 18d for inner layers which filled up the through tube 21 with conductive paste is produced. And only predetermined distance is detached, green sheet 18c for inner layers is piled up, and the predetermined number-of-sheets laminating of the green sheet 18d for inner layers is carried out to the upper and lower sides. Furthermore, green sheet 15a which filled up the through tube 21 with conductive

paste like green sheet 18d for inner layers is put on the vertical outermost layer. By sticking by pressure and calcinating this layered product, as shown in drawing 6 (b), thermistor component 12c pulled out to the both-ends side of thermistor component 12c can be obtained so that the internal electrodes 20 and 20 which the diffusion layer 13 was formed near the 4 side faces, and were formed in the interior at the external electrode 14, 14 forming faces, and parallel may be connected with the external electrodes 14 and 14.

[0034] In addition, the external electrodes 14 and 14 of the chip mold thermistors 11 and 11b When the specific resistance which uses as a principal component the oxide which makes it suitably the presentation of the thermistor components 12 and 12b, for example, consists of two or more sorts of Mn, nickel, Co, Fe, Cu, and aluminum consists of a ceramic of 200 or less ohm-cm, The printing electrode layers 14a and 14a which are substrate layers may be omitted, and deposits 14b and 14b may be formed in the thermistor components 12 and 12b with direct electrolysis plating.

[0035] The above-mentioned chip mold thermistors 11 and 11b were prepared, the chip mold thermistor which does not form the diffusion layer 13 as an example of a comparison further was prepared, and the resistance rate of change and resistance variation by electrolytic plating were investigated. The result is expressed to Table 1. In addition, an example 1 is the chip mold thermistor 11, and an example 2 is chip mold thermistor 11b.

[0036]

[Table 1]

	拡散層	メッキによる 抵抗変化率(%)	抵抗バラツキ 3 CV(%)
実施例 1	有	$\Delta R = 0.05$	6.5
実施例 2	有	$\Delta R = 0.1$	6.6
比較例 3	無	$\Delta R = 3.5$	7.5

[0037] As shown in Table 1, the chip mold thermistors 11 and 11b in which the diffusion layer 13 was formed have the resistivity change very as small as 0.05% and 0.01% by plating. Moreover, it turns out that 3valve flow coefficients which show dispersion in resistance are also small.

[0038] Next, the anti-chip box reinforcement of the chip mold thermistors 11 and 11b of examples 1 and 2 was investigated. Furthermore, the LIFE shelf test was performed and change of an elevated temperature, low temperature or the resistance in the inside of highly humid, or B constant was investigated. Similarly, it investigated and compared also

about the chip mold thermistor of the example of a comparison. In addition, a shelf test investigates the rate of a resistance value change when leaving it at RH and -40 degree C 60 degree C and [125 degrees C and] 95% for 1000 hours, respectively. The result is expressed to Table 2.

[0039]

[Table 2]

	拡散層	抗折強度 (N)	ライフ放置試験 (1000hrs.) Δ R25(%)		
			125°C 高温	60°C- 95%RH 湿中	-40°C 低温
実施例 1	有	52.6	0.7	0.7	0.3
実施例 2	有	51.2	0.8	0.7	0.3
比較例 3	無	36.3	1.3	0.8	0.4

[0040] As shown in Table 2, anti-chip box reinforcement is 51.2N and 52.6N, and the chip mold thermistors 11 and 11b in which the diffusion layer 13 was formed improved 40% or more from 36.3 Ns of a chip mold thermistor without a diffusion layer. Moreover, the chip mold thermistors 11 and 11b with which the LIFE shelf test also formed the diffusion layer had the small resistance value change, and its rate of a resistance value change in an elevated temperature was especially smaller than the chip mold thermistor without a diffusion layer.

[0041] This is because the diffusion layer 13 raised the mechanical strength of the thermistor components 12 and 12b and prevented the corrosion of the thermistor components 12 and 12b by electrolytic plating.

[0042]

[Effect of the Invention] As stated above, by forming the diffusion layer of a high specific resistance inorganic substance near the thermistor component outside surface, the chip mold thermistor concerning this invention can prevent the change in resistance by the corrosion of the component at the time of electrolytic plating, and corrosion, and can prevent degradation of the anti-chip box reinforcement of a component, and dependability aggravation. Furthermore, only by the printing method of construction, insulation-izing or since-izing can be carried out [high specific resistance], a thermistor component outside surface is excelled in mass-production nature, and low cost-ization can be realized.

[0043] Moreover, in invention concerning claim 2, in order to form an external electrode, electrode paste is applied, since it is not burned and can form by electrolytic plating, it excels in mass-production nature and low cost-ization can be realized.

[Translation done.]

* NOTICES *

JPO and NCIP are not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3. In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the sectional view of the chip mold thermistor of the gestalt of one operation concerning this invention.

[Drawing 2] The production process of the chip mold thermistor of drawing 1 is shown, and the perspective view to which (a) expresses the laminating condition of a ceramic green sheet, and (b) are the perspective views of the chip mold thermistor with which the perspective view of the chip object before baking and (c) formed the perspective view of the thermistor component after baking, and (d) formed the external electrode.

[Drawing 3] It is the sectional view showing the modification of the thermistor component in the chip mold thermistor of this invention.

[Drawing 4] It is the decomposition perspective view of the chip mold thermistor of drawing 3 .

[Drawing 5] The production process of the chip mold thermistor of the gestalt of other operations concerning this invention is shown, and the perspective view to which (a) expresses the laminating condition of a green sheet, and (b) are the perspective views of the chip mold thermistor with which the perspective view of the chip object before baking and (c) formed the perspective view of the thermistor component after baking, and (d) formed the external electrode.

[Drawing 6] How to form an internal electrode is shown in the chip mold thermistor of drawing 5 , and the perspective view to which (a) expresses the laminating condition of a green sheet, and (b) are the perspective views of the thermistor component after baking.

[Drawing 7] It is the sectional view showing the conventional chip mold thermistor.

[Drawing 8] The perspective view of the thermistor element assembly which the production process of the conventional chip mold thermistor is shown, and (a) cut the perspective view of the thermistor element assembly which formed the glass layer in both tabular principal planes, and (b) in the shape of a strip of paper, and formed the glass layer in the cutting plane, and (c) are the perspective view of the thermistor component cut in the shape of a chip, and the perspective view of the chip mold thermistor component in which (d) external electrode was formed.

[Description of Notations]

11 11b Chip mold thermistor
12 12b Thermistor component
13 Diffusion Layer
14 External Electrode
14b Electrolysis deposit
15 Green Sheet

[Translation done.]

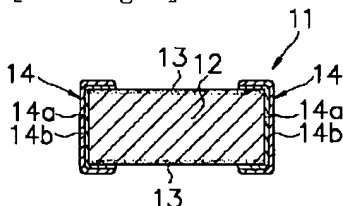
* NOTICES *

JPO and NCIPI are not responsible for any damages caused by the use of this translation.

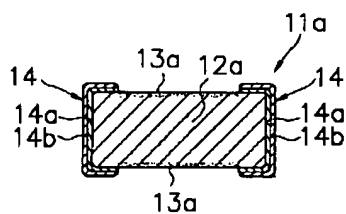
1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3. In the drawings, any words are not translated.

DRAWINGS

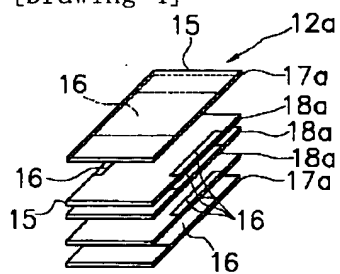
[Drawing 1]



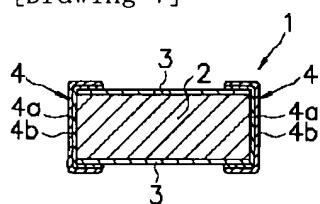
[Drawing 3]



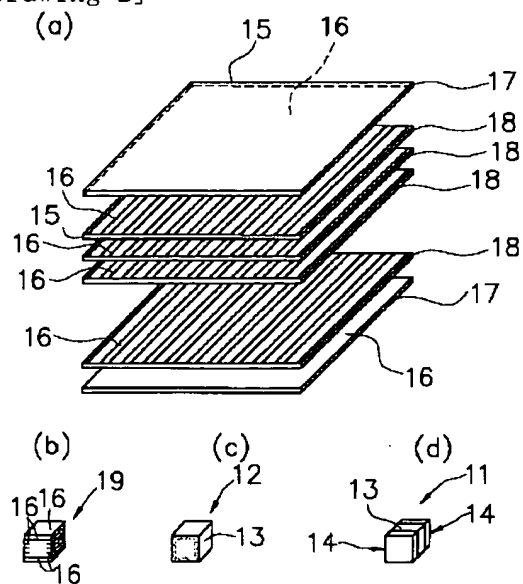
[Drawing 4]



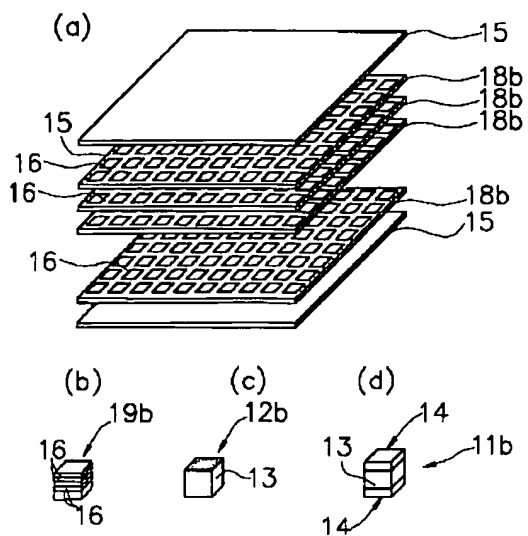
[Drawing 7]



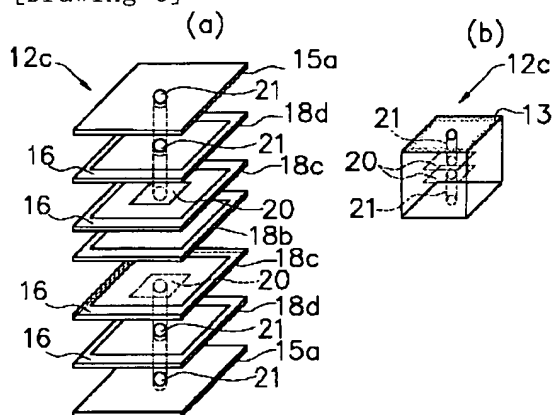
[Drawing 2]



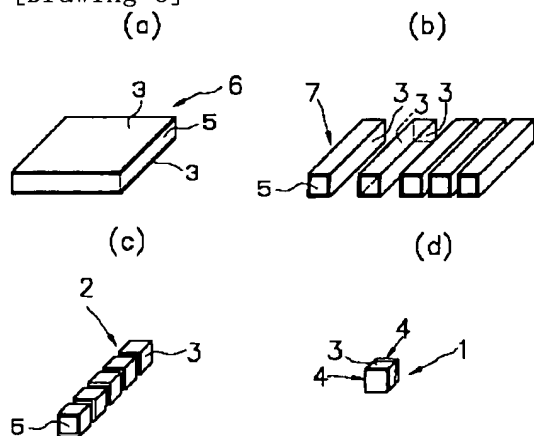
[Drawing 5]



[Drawing 6]



[Drawing 8]



[Translation done.]

**This Page is Inserted by IFW Indexing and Scanning
Operations and is not part of the Official Record**

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

☒ **BLACK BORDERS**

☐ **IMAGE CUT OFF AT TOP, BOTTOM OR SIDES**

☐ **FADED TEXT OR DRAWING**

☒ **BLURRED OR ILLEGIBLE TEXT OR DRAWING**

☐ **SKEWED/SLANTED IMAGES**

☒ **COLOR OR BLACK AND WHITE PHOTOGRAPHS**

☐ **GRAY SCALE DOCUMENTS**

☐ **LINES OR MARKS ON ORIGINAL DOCUMENT**

☐ **REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY**

☐ **OTHER:** _____

IMAGES ARE BEST AVAILABLE COPY.

As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.